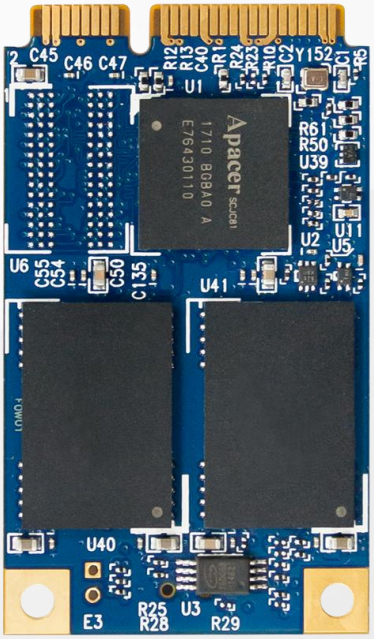
Apacer

RoHS Compliant

Serial ATA Flash Drive

SM230-300 Product Specifications

(Toshiba 15nm)



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Apacer

Specifications Overview:

- **Compliance with SATA Revision 3.2**
  - SATA 6.0 Gbps interface
  - Backward compatible with SATA 1.5 and 3.0 Gbps interfaces
  - ATA-8 command set
- **Capacity**
  - 32, 64, 128, 256, 512 GB
- **Performance***
  - Burst read/write: 600 MB/sec

  Standard:
  - Sequential read: Up to 560 MB/sec
  - Sequential write: Up to 510 MB/sec
  - Random read (4K): Up to 41,000 IOPS
  - Random write (4K): Up to 58,000 IOPS

  AES & Opal Implemented:
  - Sequential read: Up to 560 MB/sec
  - Sequential write: Up to 500 MB/sec
  - Random read (4K): Up to 39,000 IOPS
  - Random write (4K): Up to 60,000 IOPS
- **Flash Management**
  - Built-in hardware ECC
  - Global Wear Leveling
  - Flash bad-block management
  - Flash Translation Layer: Page Mapping
  - S.M.A.R.T.
  - Power Failure Management
  - Device Sleep
  - ATA Secure Erase
  - TRIM
  - Hyper Cache Technology
- **NAND Flash Type:** MLC
- **MTBF:** >1,000,000 hours
- **Temperature Range**
  - Operating:

    Standard: 0°C to 70°C

    Extended: -40°C to 85°C
  - Storage: -40°C to 100°C
- **Supply Voltage**
  - 3.3 V ± 5%
- **Power Consumption***
  - Active mode: 935 mA
  - Idle mode: 130 mA
- **Form Factor**
  - JEDEC MO-300
- **Shock & Vibration****
  - Shock: 1,500 G
  - Vibration: 15 G
- **Security**
  - Trusted Computing Group (TCG) Opal 2.0 (optional)
  - AES 256-bit hardware encryption
- **Reliability**
  - Thermal Sensor***
  - Thermal Management Technique (optional)
- **SATA Power Management Modes**
- **Write Protect Switch (optional)**
- **LED Indicators for Drive Behavior**
- **RoHS Compliant**

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.
**Non-operating
***Built-in feature for extended temperature products; optional feature for standard temperature products.

Table of Contents

1. General Descriptions

1.1 Introduction

Apacer SM230-300 is a well-balanced solid-state disk (SSD) drive with compact form factor (JEDEC MO-300) and great performance. Designed in SATA 6.0 Gbps interface, the mSATA SSD is able to deliver exceptional read/write speed, making it the ideal companion for heavy-loading embedded or server operations with space constraints for host computing systems. In regard of reliability, the drive comes with various implementations including powerful hardware ECC engine, power saving modes, wear leveling, flash block management, S.M.A.R.T., TRIM, and power failure management. Furthermore, with Advanced Encryption Standard (AES) and Trusted Computing Group (TCG) Opal support, SM230-300 ensures data security and provides users with a peace of mind knowing their data is safeguarded against unauthorized use at all times.

1.2 Capacity

Capacity specifications of SM230-300 are available as shown in Table 1-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 1-1 Capacity Specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Max LBA
32 GB	32,017,047,552	16,383	16	63	62,533,296
64 GB	64,023,257,088	16,383	16	63	125,045,424
128 GB	128,035,676,160	16,383	16	63	250,069,680
256 GB	256,060,514,304	16,383	16	63	500,118,192
512 GB	512,110,190,592	16,383	16	63	1,000,215,216

*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.
**Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

1.3 Performance

Performance of SM230-300 is listed below in Table 1-2 and 1-3.

Table 1-2 Performance Specifications (Standard)

Performance \ Capacity	32 GB	64 GB	128 GB	256 GB	512 GB
Sequential Read* (MB/s)	555	555	560	560	560
Sequential Write* (MB/s)	265	490	475	510	510
Random Read IOPS (4K)**	24,000	37,000	36,000	41,000	41,000
Random Write IOPS (4K)**	16,000	30,000	36,000	58,000	58,000

Table 1-3 Performance Specifications (AES and Opal implemented)

Capacity / Performance	32 GB	64 GB	128 GB	256 GB	512 GB
Sequential Read* (MB/s)	560	560	560	550	560
Sequential Write* (MB/s)	265	485	455	500	495
Random Read IOPS (4K)**	23,000	36,000	37,000	39,000	39,000
Random Write IOPS (4K)**	16,000	30,000	38,000	58,000	60,000

Note:
Results may differ from various flash configurations or host system setting.
*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.
**Random performance measured using IOMeter with Queue Depth 32.

1.4 Pin Assignments

Pin assignment of the SM230-300 is shown in Figure 1-1 and described in Table 1-4.

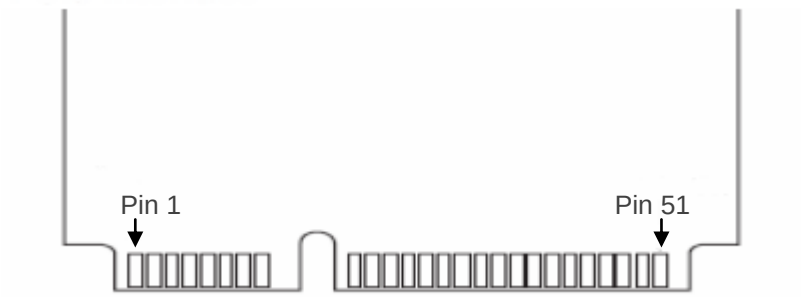


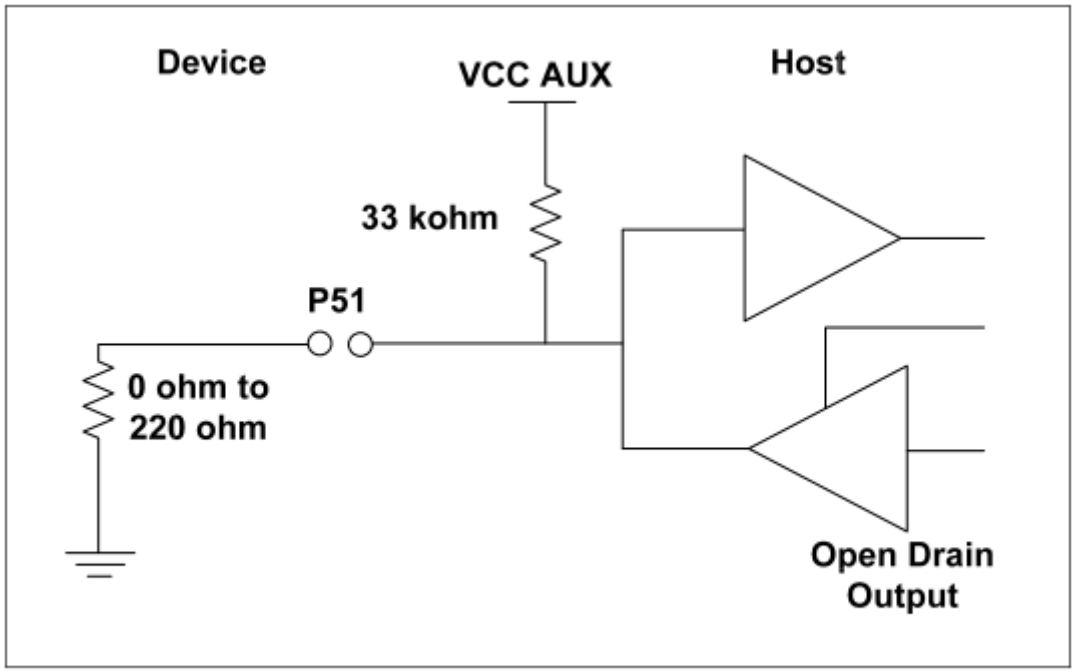
Figure 1-1 Pin Assignment

Table 1-4 Pin Assignment Description

Pin	Type	Description	Pin	Type	Description
1	Reserved	No Connect	27	GND	Ground
2	+3.3V	3.3V source	28	Reserved	No Connect
3	Reserved	No Connect	29	GND	Ground
4	GND	Ground	30	Reserved	No Connect
5	Reserved	No Connect	31	-A	Host Transmitter Differential Signal Pair
6	Reserved	No Connect	32	Reserved	No Connect
7	Reserved	No Connect	33	+A	Host Transmitter Differential Signal Pair
8	Reserved	No Connect	34	GND	Ground
9	GND	Ground	35	GND	Ground
10	Reserved	No Connect	36	Reserved	No Connect
11	Reserved	No Connect	37	GND	Ground
12	Reserved	No Connect	38	Reserved	No Connect
13	Reserved	No Connect	39	+3.3V	3.3V source
14	Reserved	No Connect	40	GND	Ground
15	GND	Ground	41	+3.3V	3.3V source
16	Reserved	No Connect	42	Reserved	No Connect
17	Reserved	No Connect	43	Device Type	No Connect
18	GND	Ground	44	DEVSLP	Device Sleep
19	Reserved	No Connect	45	Reserved	No Connect
20	Reserved	No Connect	46	Reserved	No Connect
21	GND	Ground	47	Reserved	No Connect

Pin	Type	Description	Pin	Type	Description
22	Reserved	No Connect	48	Reserved	No Connect
23	+B	Host Receiver Differential Signal Pair	49	DAS/DSS	Device Activity Signal/Disable Staggered Spin-up
24	+3.3V	3.3V Source	50	GND	Ground
25	-B	Host Receiver Differential Signal Pair	51*	Detect	0 ohm
26	GND	Ground	52	+3.3V	3.3V source

*Notes about Pin51: It is a presence detection pin that shall be connected to GND by a 0 ohm to 220 ohm Resistor on device. Please see the diagram below.



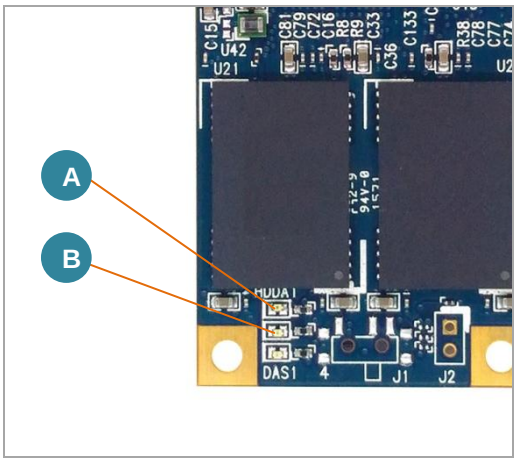
Bi-directional host-side implementation of P51 for compatibility with non-mSATA devices (informative)

1.5 LED Indicator Behavior

The behavior of the SM230-300 LED indicators is described in Table 1-5.

Table 1-5 LED Behavior

Location	Status	Description
LED A	Static	Write Protect is enabled (only available for models supporting write protection)
LED B	Static	PHY is connected



2. Software Interface

2.1 Command Set

This section defines the software requirements and the format of the commands the host sends to SM230-300. Commands are issued to SM230-300 by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register.

Table 2-1 Command Set

Code	Command	Code	Command
E5h	Check Power Mode	F6h	Security Disable Password
90h	Execute Diagnostics	F3h	Security Erase Prepare
E7h	Flush Cache	F4h	Security Erase Unit
ECh	Identify Device	F5h	Security Freeze Lock
E3h	Idle	F1h	Security Set Password
E1h	Idle Immediate	F2h	Security Unlock
91h	Initialize Device Parameters	7Xh	Seek
C8h	Read DMA	EFh	Set Features
25h	Read DMA EXT	C6h	Set Multiple Mode
60h	Read FPDMA Queued	E6h	Sleep
47h	Read Log DMA EXT	B0h	S.M.A.R.T.
2Fh	Read Log EXT	E2h	Standby
C4h	Read Multiple	E0h	Standby Immediate
20 or 21h	Read Sector(s)	CAh	Write DMA
40 or 41h	Read Verify Sector(s)	35h	Write DMA EXT
10h	Recalibrate	61h	Write FPDMA Queued
57h	Write Log DMA EXT	3Fh	Write Log EXT
C5h	Write Multiple	30h or 31h	Write Sector(s)

Table 2-2 Trusted Computing Feature Set

Code	Command	Code	Command
5Ch	Trusted Receive	5Eh	Trusted Send
5Dh	Trusted Receive DMA	5Fh	Trusted Send DMA

Note: This feature set is only applicable to products implemented with AES and Opal functions.

2.2 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our S.M.A.R.T. feature that complies with the ATA/ATAPI specifications. S.M.A.R.T. Attribute IDs shall include initial bad block count, total later bad block count, maximum erase count, average erase count, power on hours and power cycle. When the S.M.A.R.T. Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

Note: Attribute IDs may vary from product models due to various solution design and supporting capabilities.

Apacer memory products come with S.M.A.R.T. commands and subcommands for users to obtain information of drive status and to predict potential drive failures. Users can take advantage of the following commands/subcommands to monitor the health of the drive.

Code	SMART Subcommand
D0h	READ DATA
D1h	READ ATTRIBUTE THRESHOLDS
D2h	Enable/Disable Attribute Autosave
D4h	Execute Off-line Immediate
D5h	Read Log (optional)
D6h	Write Log (optional)
D8h	Enable Operations
D9h	Disable operations
DAh	Return Status

General SMART attribute structure

Byte	Description
0	ID (Hex)
1 – 2	Status flag
3	Value
4	Worst
5*-11	Raw Data

*Byte 5: LSB

SMART attribute ID list

ID (Hex)	Attribute Name
9 (0x09)	Power-on hours
12 (0x0C)	Power cycle count
163 (0xA3)	Max. erase count
164 (0xA4)	Avg. erase count
166 (0xA6)	Total later bad block count
167 (0xA7)	SSD Protect Mode (vendor specific)
168 (0xA8)	SATA PHY Error Count
175 (0xAF)	Bad Cluster Table Count
192 (0xC0)	Unexpected Power Loss Count
194 (0xC2)	Temperature
241 (0xF1)	Total sectors of write

3. Flash Management

3.1 Error Correction/Detection

SM230-300 implements a hardware ECC scheme, based on the BCH algorithm. It can detect and correct up to 76 bits error in 1K bytes.

3.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

3.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

3.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

3.5 ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

3.6 Power Failure Management

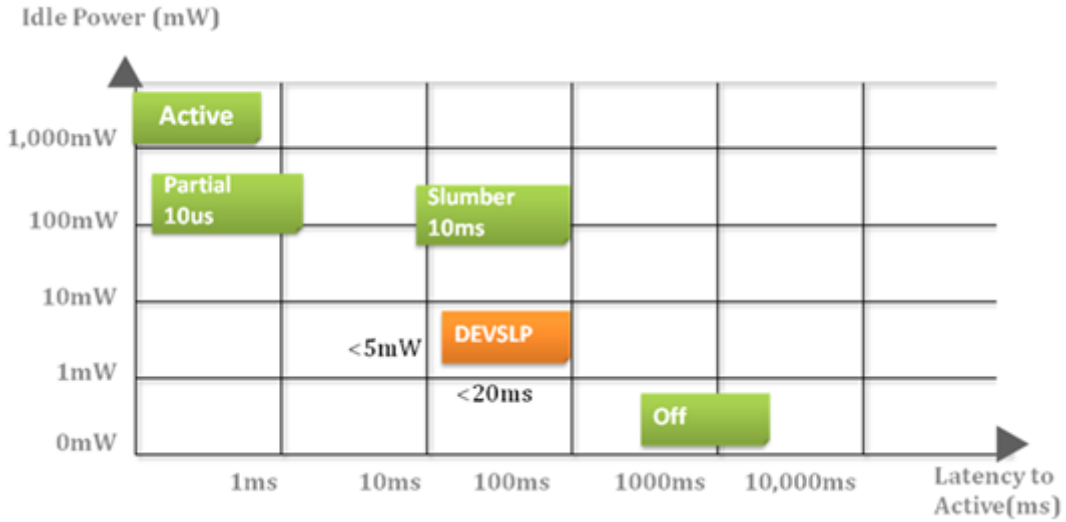
Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

3.7 TRIM

TRIM is a SATA command that helps improve the read/write performance and efficiency of solid-state drives (SSD). The command enables the host operating system to inform SSD controller which blocks contain invalid data, mostly because of the erase commands from host. The invalid will be discarded permanently and the SSD will retain more space for itself.

3.8 DEVSLP (DevSleep or DEVSLP) Mode

Device Sleep is a feature that allows SATA devices to enter a low power mode by designating pin 44 as DEVSLP signal with an aim to reducing power consumption.



Parameter	Description & Conditions	Min	Max
V_{DIn}	Tolerated input voltage.	-0.5 V	3.6 V
$V_{HAssert}$	Voltage presented to host if signal not driven low. Value specified for all allowable $I_{HAssert.}$	-	2.4 V
$I_{HNegate}$	Device current delivered to host if host driving signal low. Value specified at $V_{HNegate}$ voltage of 0 V.	-	100 uA

3.9 Hyper Cache Technology

Apacer proprietary Hyper Cache technology, a non-volatile SLC write cache, provides excellent performance to handle various scenarios in industrial use.

Using this method, a portion of the available capacity is being treated as SLC (1bit-per-cell) NAND flash memory in the Multi-Level Cell (MLC) models, two bits per cell technology, consists of a number of low and high pages. Apacer Hyper Cache Technology collects low pages for extraordinary performance, called Hyper Cache mode. And, the rest of high pages are combined together and performs normal MLC performance, called MLC mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, thus improving the write speeds drastically.

3.10 SATA Power Management

By complying with SATA 6.0 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, Tx & Rx operational
- PARTIAL: Reduces power, resumes in under 10 µs (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- HIPM: Host-Initiated Power Management
- DIPM: Device-Initiated Power Management
- AUTO-SLUMBER: Automatic transition from partial to slumber.
- Device Sleep (DevSleep or DEVSLP): PHY powered down; power consumption $\leqq$ 5 mW; host assertion time $\leqq$ 10 ms; exit timeout from this state $\leqq$ 20 ms (unless specified otherwise in SATA Identify Device Log).

Note: The behaviors of power management features would depend on host/device settings.

4. Security & Reliability Features

4.1 Advanced Encryption Standard

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. AES has been adopted by the U.S. government since 2001 to protect classified information and is now widely implemented in embedded computing applications. The AES algorithm used in software and hardware is symmetric so that encrypting/decrypting requires the same encryption key. Without the key, the encrypted data is inaccessible to ensure information security.

Notably in flash memory applications, AES 256-bit hardware encryption is the mainstream to protect sensitive or confidential data. The hardware encryption provides better performance, reliability, and security than software encryption. It uses a dedicated processor, which is built inside the controller, to process the encryption and decryption. This enormously shortens the processing time and makes it efficient.

4.2 TCG Opal (optional)

Developed by the Trusted Computing Group (TCG), an organization whose members work together to formulate industry standards, Opal is a set of security specifications used for applying hardware-based encryption to storage devices.

Hardware encryption has many advantages. First of all, it transfers the computational load of the encryption process to dedicated processors, reducing the stress on the host system's CPU. In addition, storage devices complying with Opal specifications are self-encryption devices. Opal specifications also feature boot authentication. When the drive is being accessed, the shadow MBR will request the drive password at boot. The drive will only unlock and decrypt if the correct password is supplied. The other feature is LBA-specific permissions. Users are assigned different permissions for LBA ranges created by the device administrator. Each LBA range is password-protected and can only be accessed by users with the correct key to perform permitted actions (read/write/erase).

4.3 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using a designated pin for transmission, storage device owners are able to read temperature data.

4.4 Thermal Management Technique (optional)

Thermal management technique can monitor the temperature of the SSD equipped with a built-in thermal sensor via S.M.A.R.T. commands. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device’s temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

5. Reliability Specifications

5.1 Environmental Specifications

Environmental specifications of SM230-300 product are shown in Table 5-1.

Table 5-1 Environmental Specifications

Environment	Specifications
Temperature	0°C to 70°C (Standard); -40°C to 85°C (Extended)
	-40°C to 100°C (Non-operating)
Vibration	Non-operating: Sine wave, 15(G), 10~2000(Hz), Operating: Random, 7.69(GRMS), 20~2000(Hz)
Shock	Non-operating: Acceleration, 1,500 G, 0.5 ms Operating: Peak acceleration, 50 G, 11 ms

5.2 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in SM230-300. The prediction result for SM230-300 is more than 1,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 2” method.

5.3 Certification and Compliance

SM230-300 complies with the following standards:

- CE
- FCC
- RoHS
- MIL-STD-810F

6. Electrical Specifications

6.1 Operating Voltage

Table 6-1 lists the supply voltage for SM230-300.

Table 6-1 Operating Range

Item	Range
Supply Voltage	3.3V ± 5%

6.2 Power Consumption

Table 6-2 lists the power consumption for SM230-300.

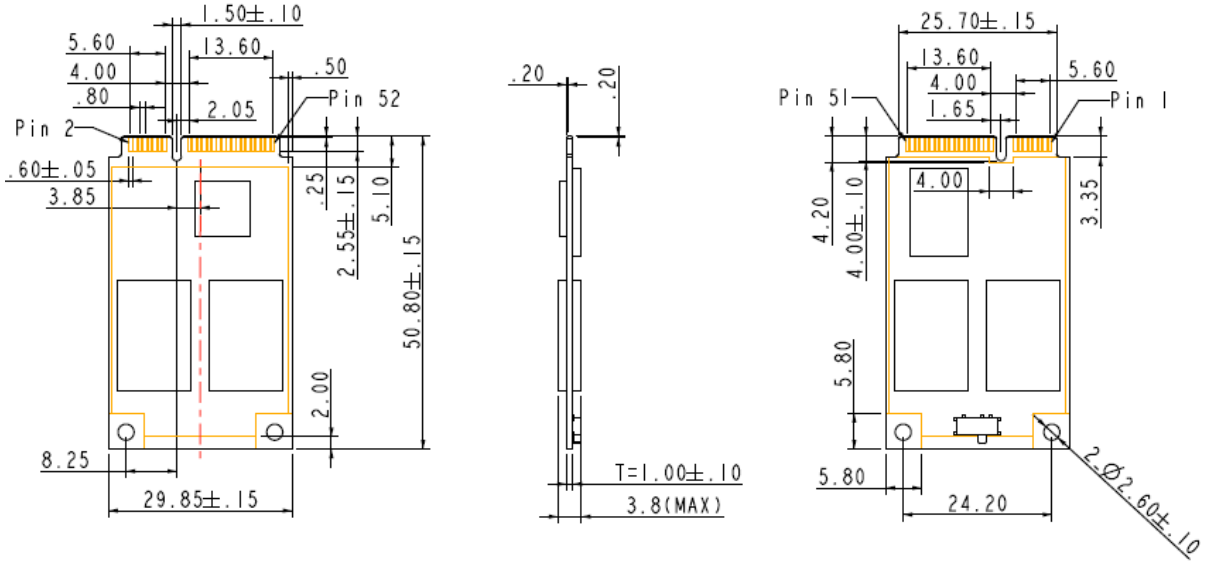
Table 6-2 Power Consumption

Capacity / Mode	32 GB	64 GB	128 GB	256 GB	512 GB
Active (mA)	660	665	705	935	770
Idle (mA)	125	125	130	125	125

Note:
*All values are typical and may vary depending on flash configurations or host system settings.
**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

7. Mechanical Specifications

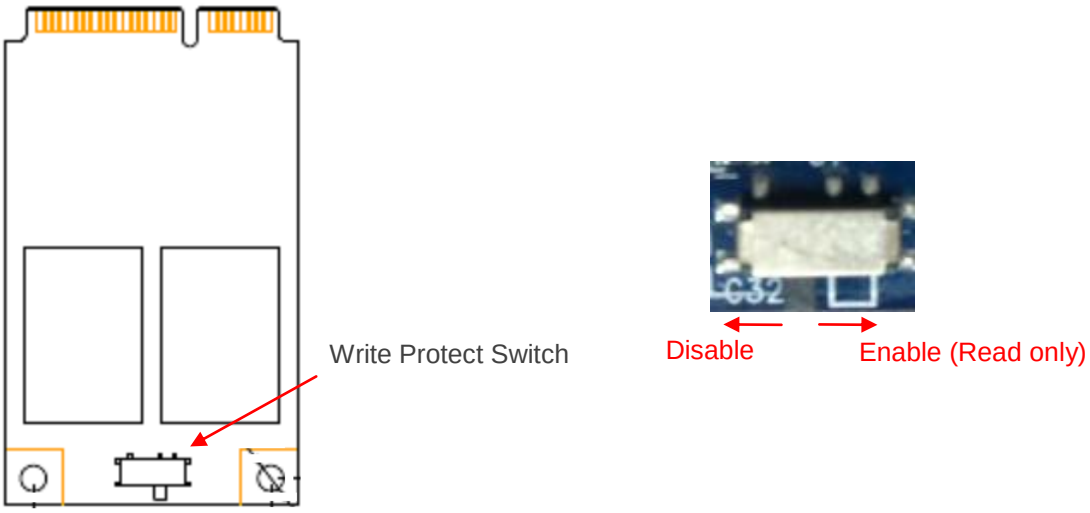
7.1 Dimensions



Unit: mm
Tolerance: ± 0.2

7.2 Write Protect Switch (optional)

Apacer implements the Virtual Write scheme that allows write commands to go through the flash controller and data temporarily stored, but no data has been actually written into the flash. Once the system is reset and rebooted, the temporarily stored data will be lost and nowhere to be found in the system. Since the Virtual Write scheme runs at device level, it requires no software or driver installation and is independent from the host OS.

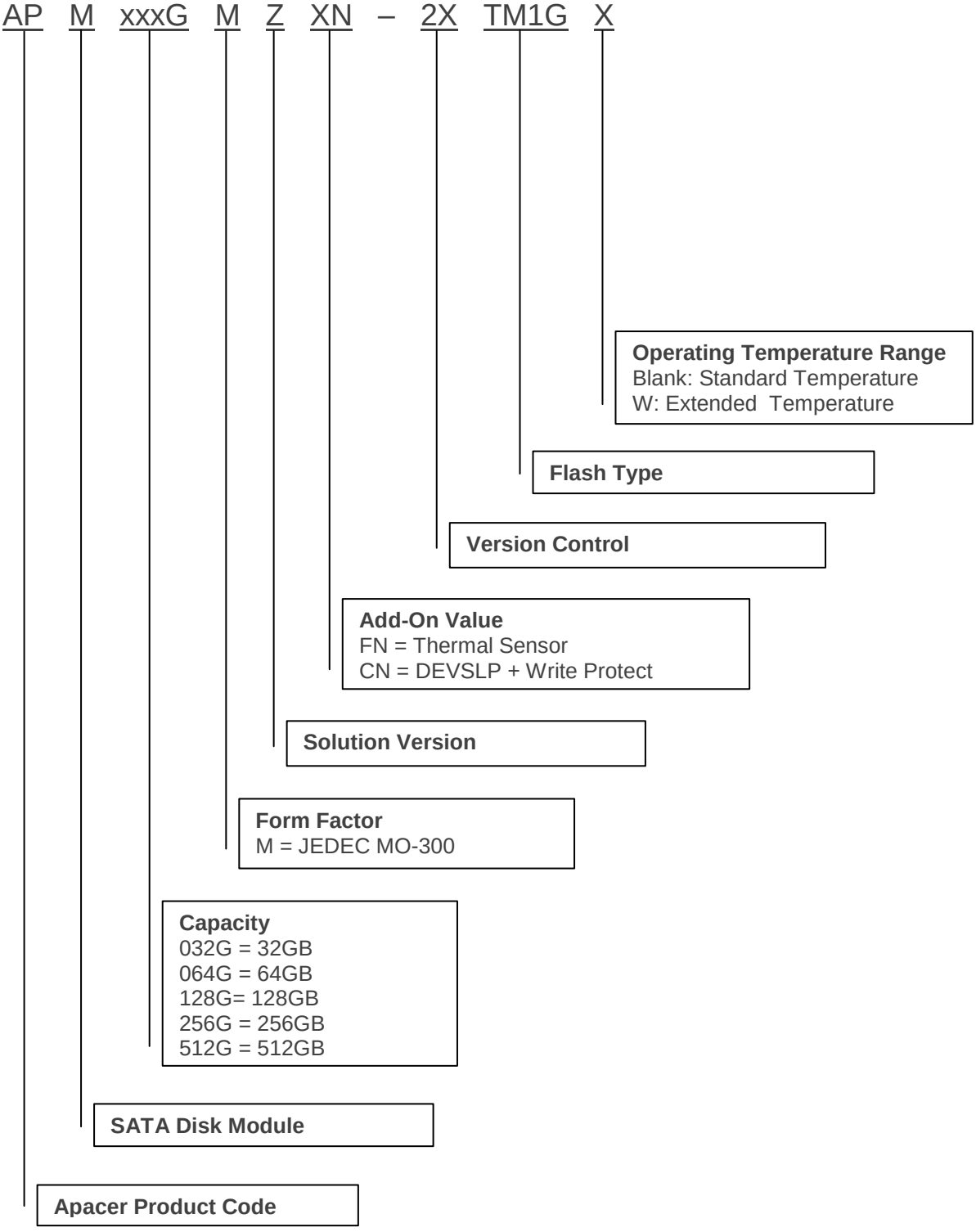


Note: Write Protect is optional and the image is for reference only.

8. Product Ordering Information

8.1 Product Code Designations

AP M xxxG M Z XN – 2X TM1G X



8.2 Valid Combinations

8.2.1 Standard

Capacity	Standard Temperature	Extended Temperature
32GB	APM032GMZFN-2BTM1G	APM032GMZFN-2BTM1GW
64GB	APM064GMZFN-2BTM1G	APM064GMZFN-2BTM1GW
128GB	APM128GMZFN-2BTM1G	APM128GMZFN-2BTM1GW
256GB	APM256GMZFN-2BTM1G	APM256GMZFN-2BTM1GW
512GB	APM512GMZFN-2BTM1G	APM512GMZFN-2BTM1GW

8.2.2 With AES/Opal Function (optional)

Capacity	Standard Temperature	Extended Temperature
32GB	APM032GMZFN-2HTM1G	APM032GMZFN-2HTM1GW
64GB	APM064GMZFN-2HTM1G	APM064GMZFN-2HTM1GW
128GB	APM128GMZFN-2HTM1G	APM128GMZFN-2HTM1GW
256GB	APM256GMZFN-2HTM1G	APM256GMZFN-2HTM1GW
512GB	APM512GMZFN-2HTM1G	APM512GMZFN-2HTM1GW

8.2.3 With Write Protect (optional)

Capacity	Standard Temperature	Extended Temperature
32GB	APM032GMZCN-2BTM1G	APM032GMZCN-2BTM1GW
64GB	APM064GMZCN-2BTM1G	APM064GMZCN-2BTM1GW
128GB	APM128GMZCN-2BTM1G	APM128GMZCN-2BTM1GW
256GB	APM256GMZCN-2BTM1G	APM256GMZCN-2BTM1GW
512GB	APM512GMZCN-2BTM1G	APM512GMZCN-2BTM1GW

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
1.0	Official release	6/25/2018
1.1	Updated 4.3 Thermal Sensor	7/9/2018
1.2	Revised part number for 32GB with extended temperature support at 8.2.3 With Write Protect (optional)	7/13/2018
1.3	Revised ECC from 40 bits to 76 bits error in 1K bytes at 3.1 Error Correction/Detection	7/20/2018
1.4	- Added a table to 3.8 DEVSLP (DevSleep or DEVSLP) Mode - Marked TCG Opal as “optional” at Security on Specifications Overview page and 4.2 TCG Opal	8/21/2018

Global Presence

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